

Errata: CS42L51 Rev. A0

Reference the CS42L51 Data Sheet

- ◆ THD+N performance of the DAC's analog output into line-level loads does not meet data sheet specification at the nominal VA supply of 2.5 V (see the table below for performance numbers).

| Data Sheet Specification | | Rev. A Silicon Performance | |
|---|------------------|----------------------------|------|
| DAC Output into $R_L = 10\text{ k}\Omega$ | Typ (VA = 2.5 V) | Typ (VA = 2.5 V) | Unit |
| THD+N | 0 dB | -78 | dB |

See control port compensation 1 below for how to improve performance:

| | VA = 2.5 V ONLY |
|------------------------------------|---|
| Control Port Compensation 1 | <p>To meet data sheet specification:</p> <ol style="list-style-type: none"> 1. Write 0x99 to register 0x00. 2. Write 0x8C to register 0x2B. 3. Write 0xD5 to register 0x38. 4. Write 0x00 to register 0x00. |

- ◆ THD+N performance of the ADC's analog input (PGA to ADC) in Double-Speed Mode (DSM) at a sample rate of $F_s = 96\text{ kHz}$, is -79 dB and -81 dB at the nominal VA supply of 1.8 V and 2.5 V, respectively. See control port compensation 2 below for how to improve performance (only valid with 1000 pF on pins AFILTA and AFILTB):

| | VA = 1.8 V | VA = 2.5 V |
|------------------------------------|--|--|
| Control Port Compensation 2 | <p>For -85 dB THD+N (DSM ONLY):</p> <ol style="list-style-type: none"> 1. Write 0x99 to register 0x00. 2. Write 0x2E to register 0x31. 3. Write 0x8F to register 0x33. 4. Write 0xB7 to register 0x35. 5. Write 0x09 to register 0x37. 6. Write 0x00 to register 0x00. | <p>For -85 dB THD+N (DSM ONLY):</p> <ol style="list-style-type: none"> 1. Write '1'b to bit 7 in register 0x02. 2. Write 0x99 to register 0x00. 3. Write 0x2E to register 0x31. 4. Write 0xDF to register 0x33. 5. Write 0xB7 to register 0x35. 6. Write 0x0A to register 0x37. 7. Write 0x00 to register 0x00. |

- ◆ To maintain PGA reliability for all modes of operation, the following writes to the control port are necessary (ONLY when *not* implementing Control Port Compensation 2 above):

| | |
|------------------------------------|--|
| Control Port Compensation 3 | <p>If Control Port Compensation 2 is <i>not</i> implemented:</p> <ol style="list-style-type: none"> 1. Write 0x99 to register 0x00. 2. Write 0xFF to register 0x33. 3. Write 0x00 to register 0x00. |
|------------------------------------|--|

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- ◆ ESD Protection passes after exposure to a Human Body Model ESD pulse up to 1 kV, meeting classification 1C of the JESD22-A114 standard.
- ◆ ESD Protection passes after exposure to a Machine Model ESD pulse up to 50 V, meeting classification A of the JESD22-A115 standard.
- ◆ The full-scale input to the ADC (PGA bypassed), PGA and MIC is greater than the data sheet specification (see the table below for full-scale input numbers) .

| | | Data Sheet Specification | Rev. A Silicon Performance | |
|--------------------------|--------------|--------------------------|----------------------------|------|
| ADC | | Typ | Typ | Unit |
| Full-scale Input Voltage | ADC | 0.72•VA | 0.89•VA | Vpp |
| | PGA (0 dB) | 0.72•VA | 0.84•VA | Vpp |
| | MIC (+16 dB) | 0.114•VA | 0.135•VA | Vpp |
| | MIC (+32 dB) | 0.018•VA | 0.021•VA | Vpp |

- ◆ For PGA settings greater than -3 dB, the behavior of the Noise Gate is inconsistent. This effect may be inaudible.
- ◆ For PGA settings greater than -3 dB with the SOFT bit enabled, the ramp rate for the ADC's mute is different between channels. This effect may be inaudible.
- ◆ The Hardware Mode control, DEM pin 4, does not enable the de-emphasis filter.
- ◆ The de-emphasis filter clips the audio output of digital signals less than ~3 kHz and above -2.9 dBFS.
- ◆ When the DAC's zero-cross function is enabled, signal-level changes by attenuation or muting may not occur on a zero crossing.
- ◆ When the ADC's zero-cross function is enabled, signal-level changes by attenuation or muting may not occur on a zero crossing.
- ◆ The Beep Generator's "off time" does not meet data sheet specification (see the table below for the off time).

| | Data Sheet Specification | Rev. A Silicon Performance |
|--------------|---------------------------------------|---------------------------------------|
| OFFTIME[2:0] | Off Time Fs = 12, 24, 48 or 96 kHz | Off Time Fs = 12, 24, 48 or 96 kHz |
| 000 | 1.23 s | 2.46 s |
| ... | ... | ... |
| 111 | 10.8 s | 21.6 s |

- ◆ The CODEC does not enter a low power, "Stand-by" state when the PDN bit is set to '1'b. To completely power down the CODEC, the PDN_DACA, PDN_DACB and PDN bits must all be set to '1'b (see the table below for "Stand-by" implementation).

| | | Data Sheet Specification | | | | | | Rev. A Silicon Performance | | | | | | | | | | | | | |
|---|----------|--------------------------|----------|----------|----------|----------|----------|----------------------------|----------|----------|-------------|----------|----------|----------|----------|----------|----------|-----|----------|----------|-------------|
| | | Power Ctl. Registers | | | | | | Power Ctl. Registers | | | | | | | | | | | | | |
| | | 02h | | | 03h | | | 02h | | | 03h | | | | | | | | | | |
| | | PDN_DACB | PDN_DACA | PDN_PGAB | PDN_PGAA | PDN_ADCB | PDN_ADCA | PDN | PDN_MICB | PDN_MICA | PDN_MICBIAS | PDN_DACB | PDN_DACA | PDN_PGAB | PDN_PGAA | PDN_ADCB | PDN_ADCA | PDN | PDN_MICB | PDN_MICA | PDN_MICBIAS |
| 2 | Stand-by | x | x | x | x | x | x | 1 | x | x | x | 1 | 1 | x | x | x | x | 1 | x | x | x |