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## **Errata: CS5581 - Silicon revision: B0**

Reference CS5581 Data Sheet revision DS796PP1 dated March 2008.

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### **Pin 12 (VLR2) Logic Level vs. Pin 13 ( $\overline{RST}$ ) Logic Level**

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#### **Description**

The  $\overline{RST}$  pin does not initialize the device correctly if pin 12 (VLR2) is held low as pin 13 ( $\overline{RST}$ ) is driven high.

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#### **Workaround**

Pin 12 (VLR2) should be driven high (to VL) until after  $\overline{RST}$  is driven high.

The pin can then remain high. Alternatively, pin 12 can be driven to ground for a slight improvement in noise performance (0.5 dB).

### **Determining the Silicon Revision of the Integrated Circuit**

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On the front of the integrated circuit, directly under the part number, is an alpha-numeric line. Characters 5 and 6 in this line represent the silicon revision of the chip. For example, this line indicates that the chip is a "B0" revision chip:

FF AA **B0** LL YY WW

This Errata is applicable only to the B0 revision of the chip.