



10/07/02

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## **Errata: CS4205 Rev. A2**

(Reference CS4205 Data Sheet revision DS489PP2)

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### **Functional Problems**

#### *General issues*

1. The analog reference will not start if a clock is being driven into XTL\_IN before power is applied to the device. Actual application circuits must be designed so that the external clock generator does not start running before the codec is powered up.

*This problem only occurs in what is considered an invalid operational mode (outside data sheet requirements) and will not be addressed in silicon.*

2. Playback and capture at 9.6 kHz, 13.714 kHz, and 24 kHz is not supported. Selecting these rates in any of the sample rate control registers will cause the corresponding SRC to operate at the nearest supported rate (11.025 kHz, 16 kHz, and 22.05 kHz respectively).

*Software workaround possible in driver.*

3. Enabling the Loudness function (reg 20h, bit D12) does not add the desired amount of bass and treble gain. Software can compensate for this problem by applying more bass and treble gain using the Master Tone Register (Index 08h).

*Software workaround possible in driver.*

4. If the PCM input channel of the Signal Processing Engine receives data from the DAC SRC (VRA=1), the right channel data will lag the left channel data by one frame.

*This problem occurs only in digital centric mode and only if the playback SRC is active. Even in this case, the one frame delay is unnoticeable to the human ear as it corresponds to about 1/4" (or 7 mm) in spatial lag.*

#### *Powerdown issues*

5. During PR4+PR5, a GPIO wakeup event will drive SDATA\_IN 'high'. Software should disable GPIO interrupts before entering PR4+PR5.

*Software workaround possible in driver.*

6. During PR5 and PR4+PR5, SCLK is driven 'high'. Software should disable SCLK (clear SDSC bit in reg 6Ah) or the serial data port (clear SDEN bit in reg 6Ah) before entering PR5 or PR4+PR5.

*Software workaround possible in driver.*

7. During primary PR4, SDO2 and SDO1 keep transmitting the last serial data sample if the source of the serial data is the AC-link (SDOS=00 in reg 5Eh). Software can prevent this problem if it disables the serial data port (clear SDEN bit in reg 6Ah) before entering primary PR4.

*Software workaround possible in driver.*

8. During secondary PR4 sleep state, the serial data port clocks (LRCLK, and SCLK) will be driven to last active state instead of 'low'. Software can prevent this problem if it disables the serial data port (clear SDEN bit in reg 6Ah) before entering secondary PR4 sleep state.

*Software workaround possible in driver.*

## **Performance Problems**

### ***Pops and clicks***

9. Clearing PR1 causes a click if the DAC path is unmuted. Software can prevent this problem by muting the PCM Out Volume (reg 18h) (if DDM=0) or muting the Master Out Volume (reg 02h) and Mono Out Volume (reg 06h) (if DDM=1) before clearing PR1.

*Software workaround possible in driver.*

10. Clearing PR3 and RESET# low-high transition cause a pop.

*An applications level workaround is possible by not loading Vrefout capacitively.*

### ***Analog performance***

11. The MIC1/2 inputs show increased distortion above -2 dBV (0.8 Vrms) input voltage.

*PC 99 and PC 2001 THD+N compliance testing is done at -3 dB input level, so this problem will not affect certification.*

### ***Current consumption***

- 12a. The clocking supply current (DVdd1) is too high during PR4+PR5 (2.7 mA) and during RESET (0.5 mA).

12b. The analog supply current (AVdd1) is too high during PR3 (1.9 mA).

12c. The analog (AVdd1) and clocking (DVdd1) supply currents are too high when setting PR3 and PR4 and PR5 simultaneously. Software can prevent this problem by first setting PR3, waiting for about 500 ms and then setting PR4+PR5.

*Software workaround possible in driver.*

### ***Digital signal quality***

13. BIT\_CLK jitter is too high (about 2.5 ns).

*There is sufficient setup time margin to compensate for this problem.*

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